To store and retrieve information using a memory, data is asserted on multiple data lines by a data source device. In a purely synchronous system, data output and capture are referenced to a common free-running system clock. The maximum data rate for such as a system, however, is reached when the sum of output access time and flight time approaches the bit time (the reciprocal of the data rate). Although generating delayed clocks for early data launch and/or late data capture allows for increased data rates, such techniques do not account for movement of the data valid window (DVW, or data eye) relative to any fixed clock signal, for example, due to changes in temperature, voltage, or loading.

Please replace Paragraph **[0027]** with the following:

The guardband intervals are suitably separated from the DVW 300 nominal midpoint by any duration selected to identify variation in the DVW 300 characteristics and correspond to a desired DVW 300 duration. In the present embodiment, the guardbands are set approximately, or slightly less than, half the expected duration of the DVW 300 from the nominal midpoint. Consequently, the first tap corresponds to a delay immediately after the leading edge 310 of the DVW 300 (the nominal leading edge), and the third tap similarly corresponds to a delay immediately before the trailing edge 312 of the DVW 300 (the nominal trailing edge). The delay associated with each tap may be adjustably programmed, such as to correspond to an adjusted midpoint of the DVW 300 as it moves, for example, due to temperature and/or voltage variations.

Please replace Paragraph **[0028]** with the following:

The latch circuit 412 receives data from the data source 106 and latches input data at its output upon receipt of a delay clock

signal from the delay circuit 410. The latch circuit 412 may comprise any suitable system for asserting and holding data upon receipt of a delay clock signal. In the present embodiment, each output of the delay circuit 410 is connected to a corresponding latch circuit 412. Each latch circuit 412 comprises a circuit for latching an input value at an output upon assertion of a latch signal. Each latch circuit 412 may comprise a circuit having a data input, a clock input for the latch signal, and an output, such as a flip-flop. The data input is connected to the data source 106, for example, via a buffer 418. In the present embodiment, the data source 106 is the memory module 210. The clock input is connected to the corresponding tap outputs of the delay circuit 410, and the latch circuit output is connected to the compare circuit 414. The output of the center latch circuit is also connected to the data destination 106. When the various taps of the delay circuit 410 assert their respective delay clock signals, each latch circuit 412 is activated to capture the input data received by the latch circuit 412 when the delay clock signal is asserted. Thus, each latch circuit 412 captures data received from the data source 106 at different times, such as the midpoint and the leading and trailing edges 310, 312 of the timing and/or data signal.

Please replace Paragraph **[0035]** with the following:

After the memory system 104 has been calibrated, the system may be adjusted at any desired time. While the memory system 104 operates, the adaptive timing system 214 may check the DVW 300 to determine whether the midpoint of the DVW 300 has drifted. The adaptive timing system 214 may check the DVW 300 at any time, for example, continuously, at periodic intervals, or upon expiration of a timer. Further, the adaptive timing system

214 may adjust the nominal midpoint and leading and trailing edges 310, 312 in the event of drift. If the memory controller 212 operates with multiple memory modules 210 or sections, the adaptive timing system 214 may perform an adjustment process for each memory module 210A, B or section of memory.

Please replace Paragraph **[0039]** with the following:

The present embodiment is described in conjunction with a delay circuit 410 having three taps, one for the nominal midpoint and two for the nominal leading and trailing edges 310, 312 of the DVW 300. Additional taps may be provided, however, to collect data about other portions of the data signal. For example, additional taps may be assigned to intervals between the midpoint and the edges 310, 312 of the DVW 300 and may be similarly connected to compare circuits 414. The data collected by latch circuits 412 connected to the additional taps may be used to identify changes in the DVW 300 as well as the rate at which the changes in the DVW 300 are occurring.

Applicant has included as an attachment to this Amendment a clean version of paragraphs [0002], [0003], [0027], [0028], [0035], and [0039].

Clean version of paragraph [0002]:

Many electronic systems and virtually every computer includes a memory to store information. For temporary storage, many systems use random access memory (RAM) for high access speed and low cost. Several types of RAM and other memory devices have been and continue to be developed as computers and other electronic systems evolve.

Clean version of paragraph [0003]:

To store and retrieve information using a memory, data is asserted on multiple data lines by a data source device. In a purely synchronous system, data output and capture are referenced to a common free-running system clock. The maximum data rate for such a system, however, is reached when the sum of output access time and flight time approaches the bit time (the reciprocal of the data rate). Although generating delayed clocks for early data launch and/or late data capture allows for increased data rates, such techniques do not account for movement of the data valid window (DVW, or data eye) relative to any fixed clock signal, for example, due to changes in temperature, voltage, or loading.

Clean version of paragraph [0027]:

The guardband intervals are suitably separated from the DVW 300 nominal midpoint by any duration selected to identify variation in the DVW 300 characteristics and correspond to a desired DVW 300 duration. In the present embodiment, the guardbands are set approximately, or slightly less than, half the expected duration of the DVW 300 from the nominal midpoint. Consequently, the first tap corresponds to a delay immediately after the leading edge 310 of the DVW 300 (the nominal leading edge), and the third tap similarly corresponds to a delay immediately before the trailing edge 312 of the DVW 300 (the nominal

trailing edge). The delay associated with each tap may be adjustably programmed, such as to correspond to an adjusted midpoint of the DVW 300 as it moves, for example, due to temperature and/or voltage variations.

Clean version of paragraph [0028]:

The latch circuit 412 receives data from the data source 106 and latches input data at its output upon receipt of a delay clock signal from the delay circuit 410. The latch circuit 412 may comprise any suitable system for asserting and holding data upon receipt of a delay clock signal. In the present embodiment, each output of the delay circuit 410 is connected to a corresponding latch circuit 412. Each latch circuit 412 comprises a circuit for latching an input value at an output upon assertion of a latch signal. Each latch circuit 412 may comprise a circuit having a data input, a clock input for the latch signal, and an output, such as a flip-flop. The data input is connected to the data source 106, for example, via a buffer 418. In the present embodiment, the data source 106 is the memory module 210. The clock input is connected to the corresponding tap outputs of the delay circuit 410, and the latch circuit output is connected to the compare circuit 414. The output of the center latch circuit is also connected to the data destination 106. When the various taps of the delay circuit 410 assert their respective delay clock signals, each latch circuit 412 is activated to capture the input data received by the latch circuit 412 when the delay clock signal is asserted. Thus, each latch circuit 412 captures data received from the data source 106 at different times, such as the midpoint and the leading and trailing edges 310, 312 of the timing and/or data signal.

Clean version of paragraph [0035]:

After the memory system 104 has been calibrated, the system may be adjusted at any desired time. While the memory system 104 operates,

the adaptive timing system 214 may check the DVW 300 to determine whether the midpoint of the DVW 300 has drifted. The adaptive timing system 214 may check the DVW 300 at any time, for example, continuously, at periodic intervals, or upon expiration of a timer. Further, the adaptive timing system 214 may adjust the nominal midpoint and leading and trailing edges 310, 312 in the event of drift. If the memory controller 212 operates with multiple memory modules 210 or sections, the adaptive timing system 214 may perform an adjustment process for each memory module 210A, B or section of memory.

Clean version of paragraph **[0039]**:

The present embodiment is described in conjunction with a delay circuit 410 having three taps, one for the nominal midpoint and two for the nominal leading and trailing edges 310, 312 of the DVW 300. Additional taps may be provided, however, to collect data about other portions of the data signal. For example, additional taps may be assigned to intervals between the midpoint and the edges 310, 312 of the DVW 300 and may be similarly connected to compare circuits 414. The data collected by latch circuits 412 connected to the additional taps may be used to identify changes in the DVW 300 as well as the rate at which the changes in the DVW 300 are occurring.